PCN Number:	20200309001.2	**PCN Date:**	Mar. 31, 2020
Title:	Qualify UMC-F12 for c021.A Process as alternate source		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	Oct. 1, 2020	**Estimated Sample Availability:**	Date provided at sample request

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☐	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☒	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☒	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing the qualification of Wafer Fab site UMC-F12 in the c021.A process as an alternate source.

Current Fab Site			Alternate Fab Site		
Current Fab Site	**Process**	**Wafer Diameter**	**New Fab Site**	**Process**	**Wafer Diameter**
DMOS6	c021.A	300 mm	UMC-F12	c021.A	300 mm

Description	Current Fab	Alternate Fab
Gate Oxide Material	Nitrided Thin Gate Oxide	SiO2
Dielectric Material	OSG/FSG/TEOS	LK SiOC (K value = 3.1)
Metallization material, front or back side	Copper Interconnect	Front side. Interconnection: Copper RDL (Re-distribution Layer): Aluminum
Contact	NiPt	W fill with TiN barrier
Contact Via Plug	Tungsten	Cu fill with Ta barrier
Top protective layer or Passivation layer material	PO Oxide (TEOS/SiON)	SiN

Reason for Change:

Qualify c021.A to UMC-F12 as alternate source.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

None

Changes to product identification resulting from this PCN:

Current:

Current Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DMOS6	DM6	USA	Dallas

New Fab Site:

New Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
UMC-F12	**F12**	**TWN**	**Tainan**

Sample Product Shipping Label (not actual product label)

TEXAS INSTRUMENTS
MADE IN: Malaysia
2DC: 2Q:

MSL 2 /260C/1 YEAR	SEAL DT
MSL 1 /235C/UNLIM	03/29/04

OPT:
ITEM: 39
LBL: 5A (L)T0:1750

(1P) SN74LS07NSR
(Q) 2000 (D) 0336
(31T)LOT: 3959047MLA
(4W) TKY(1T) 7523483SI2
(P)
(2P) REV: (V) 0033317
(20L) CSO:SHE (21L) CCO:USA
(22L) ASO:MLA (23L) ACO:MYS

Product Affected:

DS90UB964TRGCRQ1
DS90UB964TRGCTQ1

Automotive New Product Qualification Summary

(As per AEC-Q100 and JEDEC Guidelines)

Approved 14-January-2020

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

	Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: DS90UB964TRGCRQ1
Test Group A – Accelerated Environment Stress Tests								
	HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 110C/85%RH	264 Hours	3/231/0
	UHAST	A3	JEDEC JESD22-A118	3	77	Unbiased HAST, 110C/85%RH	264 Hours	3/231/0
	TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	3/231/0
	TC-BP	A4	MIL-STD883 Method 2011	1	30	Post Temp Cycle Bond Pull	Wires	3/90/0
	PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle	1000 Cycles	N/A
	HTSL	A6	JEDEC JESD22-A103	1	45	High Temp Storage Bake 150C	1000 Hours	1/45/0
Test Group B – Accelerated Lifetime Simulation Tests								
	HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125C	1000 Hours	3/231/0
	ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 125C	48 Hours	3/2400/0
	EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	-	N/A
Test Group C – Package Assembly Integrity Tests								
	WBS	C1	AEC Q100-001	1	30	Wire Bond Shear (Cpk>1.67)	Wires	1/30/0
	WBP	C2	MIL-STD883 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires	1/30/0
	PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	-	3/30/0
	LI	C6	JEDEC JESD22-B105	1	50	Lead Integrity	-	N/A
Test Group D – Die Fabrication Reliability Tests								
	EM	D1	JESD61	-	-	Electromigration	-	Completed Per Process Technology Requirements
	TDDB	D2	JESD35	-	-	Time Dependant Dielectric Breakdown	-	Completed Per Process Technology Requirements
	HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	-	Completed Per Process Technology Requirements
	NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	Completed Per Process Technology Requirements
	SM	D5	-	-	-	Stress Migration	-	Completed Per Process Technology Requirements

	Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: DS90UB964TRGCRQ1
Test Group E – Electrical Verification Tests								
	HBM	E2	AEC Q100-002	1	3	ESD - HBM - Q100	4000 V All pins	1/3/0
	HBM	E2	AEC Q100-002	1	3	ESD - HBM - Q100	8000V RIn+[3:0] and RIN-[3:0] pins	1/3/0
	CDM	E3	AEC Q100-011	1	3	ESD - CDM - Q100	1000 V	1/3/0
	LU	E4	AEC Q100-004	1	6	Auto Latch-up	Ta(max)	1/6/0
	ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67	3/90/0

A1 (PC): Preconditioning:
Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I) : -40°C to +85°C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST

Green/Pb-free Status:
Qualified Pb-Free(SMT) and Green

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